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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,903	04/05/2004	Derek Hing Sang Tam	1875.4220001	2630

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STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
COX, CASSANDRA F	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/816,903	TAM ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 11-14* is/are rejected.

7)☒ Claim(s) *5 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 10 is objected to because of the following informalities: In line three of the claim, the reference to the third NMOS transistor should be deleted. The width/length ratio of the third transistor cannot be double the width/length ratio of itself. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-7, and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Laws (U.S. Patent No. 6,664,824).

In reference to claim 1, Laws discloses in Figure 3 a differential frequency doubler circuit (40), comprising: differential input terminals (43, 44); differential output terminals (49, 50); a frequency doubler module (41, 42) coupled between the differential input terminals (43, 44) and a first one (49) of the differential output terminals; and a phase reversal module (46) coupled between the frequency doubler module and a second one (50) of the differential output terminals. The same applies to claim 11.

In reference to claim 2, Laws discloses in Figure 3 wherein the frequency doubler module (41, 42) receives a differential input signal (from the VCO 55) and generates a first output signal (49) having a frequency that is double a frequency of the differential input signal, and wherein the phase reversal module generates a second output signal (50) that is substantially equal in amplitude and opposite in phase to the first output signal (49), wherein the first (49) and second (50) output signals form a differential output signal having the frequency that is double a frequency of the differential input (this is seen to be an inherent outcome of this frequency doubler).

In reference to claim 3, because the claimed structure is fully met by Laws, the recited function or "result" limitations "wherein said differential output signal has a duty ratio that is substantially equal to a duty ratio of the input signal" will necessarily be inherent in Laws, as held by the court in In re Best, 195 USPQ 430.

In reference to claim 4, Laws discloses in Figure 3 wherein the phase reversal module comprises a transistor (46) including a gate terminal (the base terminal is seen to be equivalent to a gate terminal) coupled to a fixed voltage (BIAS) and a source terminal (the emitter is seen to be equivalent to a source terminal) having a terminal voltage that varies with an output of the frequency doubler. The same applies to claim 12.

In reference to claim 6, Laws further discloses in Figure 3 a DC bias module (45, 47, 48) coupled between the frequency doubler (41, 42) and the phase reversal module (46).

In reference to claim 7, Laws discloses in Figure 3 that the frequency doubler module comprises a first transistor (41, wherein the npn transistor shown is interchangeable with an NMOS transistor, of which fact official notice is taken) including a gate terminal (this is seen to be the base terminal) coupled to a first one (43) of the differential input terminals, a drain terminal (this is seen to be equivalent to the collector) coupled to a first one (49) of the differential output terminals, and a source terminal (this is seen to be equivalent to the emitter); and a second transistor (42, wherein the npn transistor shown is interchangeable with an NMOS transistor, of which fact official notice is taken) including a gate terminal (this is seen to be the base terminal) coupled to a second one (44) of the differential input terminals, a drain terminal (this is seen to be equivalent to the collector) coupled to a first one (49) of the differential output terminals, and a source terminal (this is seen to be equivalent to the emitter) coupled to the first transistor source terminal; wherein the phase reversal module transistor comprises a third transistor (46, wherein the npn transistor shown is interchangeable with an NMOS transistor, of which fact official notice is taken) including a drain terminal (this is seen to be equivalent to the collector) coupled to a second one (50) of the differential output terminals, and a source terminal (this is seen to be equivalent to the emitter) coupled to the source terminals of the first and second transistors (through capacitor 48), and a gate terminal (this is seen to be equivalent to the base) coupled to the fixed voltage (BIAS).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Westwick et al. (U.S. Patent No. 5,945,878).

In reference to claim 12, Westwick discloses in Figure 1 a method for controlling a transistor to generate a current that is opposite in phase to a reference current, comprising: coupling a gate terminal of the transistor (M2) to a fixed voltage; varying a source terminal of the transistor (M2) with the reference current; whereby the transistor (M2) generates a current (I_{OUT2}) that is substantially equal in amplitude and opposite in phase to the reference current (I_{OUT1}).

5. Claims 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamane et al. (U.S. Patent No. 4,813,048).

In reference to claim 13, Yamane discloses in Figure 6 a method for controlling a transistor to generate a current that is opposite in phase to a reference current, comprising: coupling a source terminal of the transistor (Q7) to a fixed voltage (-V); varying a gate terminal of the transistor (Q7) with the reference current; whereby the transistor (Q7) generates a current that is substantially equal in amplitude and opposite in phase to the reference current (see Figure 10).

In reference to claim 14, Yamane discloses in Figure 6 wherein the varying of the gate terminal comprises varying a gate terminal of the transistor (Q7) under control of an operational amplifier (OP2) in a feedback loop.

Allowable Subject Matter

6. Claims 5 and 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claims 5, 8, and 10 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 6 wherein the phase reversal module comprises a transistor (306) including a source terminal coupled to a fixed voltage and a gate terminal voltage that varies with an output of the frequency doubler in combination with the rest of the limitations of the base claims and any intervening claims. Claim 9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the width/length ratio of the third NMOS (306) is approximately double a width/length ratio of the first (302) and second (304) NMOS transistors in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

June 10, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800